IN THE CLAIMS:

Claims 1-27 have been canceled. New claims 28-47 have been added. Please note that all claims currently pending and under consideration in the referenced application are shown below. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claims 1-27 (Canceled).

28. (New) An integrated circuit comprising:

a semiconductor die;

a plurality of memory cells arranged in at least one array formed on the semiconductor die, each of the plurality of memory cells including at least one container-configured capacitor having a storage node including a roughened outer surface in a substantially vertical dimension with respect to the semiconductor die;

a word line formed substantially below the at least one container-configured capacitor, wherein each of the plurality of memory cells couples to the word line; and

a digit line formed substantially above the at least one container-configured capacitor, wherein each of the plurality of memory cells couples to the digit line.

29. (New) The integrated circuit of claim 28, further comprising circuitry formed on the semiconductor die and coupled to the memory cells for permitting data to be written to and read from the plurality of memory cells.

30. (New) The integrated circuit of claim 28, wherein the memory cells are formed with a minimum capable photolithographic feature dimension, and a single one of the memory cells consumes an area of no more than eight times the square of the minimum capable photolithographic feature dimension.

31. (New) The integrated circuit of claim 28, further comprising a conductive isolation line formed substantially below the at least one container-configured capacitor, wherein each of the plurality of memory cells couples to the conductive isolation line.

32. (New) The integrated circuit of claim 28, further comprising a dielectric layer formed substantially above the digit line.

33. (New) The integrated circuit of claim 28, further comprising a second digit line, wherein the second digit line and the digit line are separated by an insulated dielectric material.

34. (New) The integrated circuit of claim 28, wherein the memory cells are dynamic random access memory cells.

35. (New) The integrated circuit of claim 28, wherein at least 16,000,000 to 17,000,000 functional and operably addressable memory cells are formed on the semiconductor die.

36. (New) The integrated circuit of claim 35, wherein all the functional and operably addressable memory cells formed on the semiconductor die have a combined area on the semiconductor die that is no greater than 14 mm^2.

37. (New) A method of forming an integrated circuit, the method comprising:
forming a memory cell with at least one container-configured capacitor;
roughening an outer surface of the container-configured capacitor; and
attaching the container-configured capacitor to a substrate such that the outer surface of the container-configured capacitor is in a substantially vertical direction in relation to the substrate.

38. (New) The method of claim 37, further comprising forming a word line substantially below the container-coupled capacitor and coupling the word line with the memory cell.

39. (New) The method of claim 37, further comprising forming a digit line substantially above the container-coupled capacitor and coupling the digit line with the memory cell.

40. (New) The method of claim 37, further comprising forming a conductive isolation line substantially below the at least one container-configured capacitor and coupling the conductive isolation line with the memory cell.

41. (New) The method of claim 37, wherein forming a memory cell with at least one container-configured capacitor comprises:
disposing an insulative silicon dioxide material over the substrate; and
disposing a conductively doped amorphous silicon material over the insulative silicon dioxide material.

42. (New) The method of claim 41, wherein forming a memory cell with at least one container-configured capacitor further comprises disposing a dielectric material over the conductively doped amorphous silicon material.

43. (New) The method of claim 42, wherein forming a memory cell with at least one container-configured capacitor further comprises disposing a conductively doped polysilicon material over the dielectric material.

44. (New) The method of claim 37, wherein roughening the outer surface of the container-configured capacitor comprises raising the substrate temperature to an annealing temperature to convert the outer surface from a first roughness level to a second roughness level.

45. (New) The method of claim 41, wherein roughening the outer surface of the container-configured capacitor comprises:
providing a plurality of discontinuous silicon particles over the conductively doped amorphous

silicon material; and

raising the substrate temperature to an annealing temperature to convert the outer surface from a first roughness level to a second roughness level.

46. (New) The method of claim 37, further comprising forming at least one field oxide region on the substrate.

47. (New) The method of claim 39, wherein forming at least one field oxide region comprises:

providing at least one masking block to a top surface of the substrate;

disposing a silicon material over the at least one masking block;

oxidizing the silicon material and the substrate; and

removing the at least one masking block from the substrate.